Amendment to the Specification:

Rewrite the second full paragraph on page 6 to read as follows:

A1

The basic architecture of an example of a processor, or microprocessor, according to the invention will now be described. Processor 100 is a programmable fixed point DSP core with variable instruction length (8 bits to 48 bits) offering both high code density and easy programming. Architecture and instruction set are optimized for low power consumption and high efficiency execution of DSP algorithms as well as pure control tasks, such as for wireless telephones, for example. Processor 100 includes emulation and code debugging facilities.

Rewrite the third full paragraph on page 6 to read as follows:

A2

Figure 1 is a schematic overview of a digital system 10 in accordance with an embodiment of the present invention. The digital system includes a processor 100 and a processor backplane 20. In a particular example of the invention, the digital system is a Digital Signal Processor System 10 implemented in an Application Specific Integrated Circuit (ASIC). In the interest of clarity, Figure 1 only shows those portions of ~~microprocessor~~ processor 100 that are relevant to an understanding of an embodiment of the present invention. Details of general construction for DSPs are well known, and may be found readily elsewhere. For example, U.S. Patent 5,072,418 issued to Frederick Boutaud, et al, describes a DSP in detail and is incorporated herein by reference. U.S. Patent 5,329,471 issued to Gary Swoboda, et al, describes in detail how to test and emulate a DSP and is incorporated herein by reference. Details of portions of ~~microprocessor~~ processor 100 relevant to an embodiment of the present invention are explained in sufficient detail herein below, so as to enable one of ordinary skill in the microprocessor art to make and use the invention.

Rewrite the second full paragraph on page 7 to read as follows:

A3

A description of various architectural features and a description of a complete set of instructions of the microprocessor of Figure 1 is provided in co-assigned application Serial No. 09/410,977 ~~(TI-28433)~~, now U.S. Patent No. 6,658,578, which is incorporated herein by reference.

Rewrite the third full paragraph on page 7 to read as follows:

A4

As shown in Figure 1, processor 100 forms a central processing unit (CPU) with a processor core 102 and a memory ~~interface~~ management unit 104 for interfacing the processor core 102 with memory units external to the processor core 102.

Rewrite the fourth full paragraph on page 7 to read as follows:

A5

Processor backplane 20 comprises ~~a~~ ASIC backplane ~~bus~~ 22, which is a bus to which the memory management unit 104 of the processor is connected. Also connected to the ASIC backplane ~~bus~~ 22 is an instruction memory 24, peripheral devices 26 and an external interface 28.